Listing of Claims

1.   (Currently Amended) A method for managing ~~reducing overall network delays and~~ ~~efficient management of~~ ATM resources, ~~the method~~ comprising:

passing an ATM cell received by an ATM switch to a cell processing circuit;

adding an α Byte of routing information to a ~~front portion of an ATM cell~~ header of the ATM cell ~~when processing a cell having end destination information, so that the~~ ~~destination information is not lost, allowing interfacing between each network element to~~ ~~perform cell processing and routing operations with a single cell switching operation;~~

removing the routing information added to the ATM cell after processing by the cell processing circuit; and

routing the ATM cell to a destination based on the removed routing information, wherein the routing information is added after the ATM cell passes through the ATM switch and wherein the ATM cell is routed along a signal path that bypasses the ATM switch after the routing information is removed.

2.   (Currently Amended) A method of switching an asynchronous transfer mode (ATM) cell having a payload portion and a header portion comprising:

passing the ATM cell through an ATM switch;

adding an information field to ~~before~~ the header portion of the ATM cell;

processing the ATM cell ~~having a total of more than 53 bytes~~; and

forwarding the ATM cell <u>to a destination</u> after the information field is removed, <u>the ATM cell forwarded to said destination along a signal path that bypasses the ATM switch</u>.

3.   (Currently Amended) The method of claim 2, wherein the ATM cell during processing has (53+ α) bytes, and α <u>corresponds to</u> ~~is~~ a size of the information field.

4.   (Canceled)

5.   (Currently Amended) A method of processing an asynchronous transfer mode (ATM) cell comprising:

~~performing cell~~ switching ~~on~~ a received ATM cell <u>through an ATM switch</u>;

adding routing information in ~~front of~~ a header of the ATM cell that has been switched; and

forwarding the ATM cell according to the added routing information without any further cell switching <u>through the ATM switch, the ATM cell being forwarded along a signal path that bypasses the ATM switch</u>.

6.   (Original) The method of claim 5, wherein the received ATM cell has a size of 53 bytes.

7.   (Original) The method of claim 6, wherein the added routing information has a

size of 1 byte.

8.   (Original) The method of claim 7, wherein the forwarded ATM cell has a size of

53 bytes, after the 1 byte routing information has been removed.

9.   (Currently Amended) The method of claim 5, further <u>comprising</u> ~~including a step~~

~~of~~ processing the ATM cell before forwarding.

10.   (Currently Amended) The method of claim 9, wherein <u>said</u> ~~the~~ processing ~~step~~

comprises [[a]] changing of an ATM adaptation layer (AAL) type or a changing of payload

information.

11.   (Currently Amended) An asynchronous transfer mode (ATM) cell switching

system comprising:

        a first memory to receive and store an ATM cell to be handled;

        a cell switching unit to receive the ATM cell stored in the first memory, and to

assign an appropriate path for the ATM cell to be forwarded ~~to; and~~

        <u>a second memory to receive and store the ATM cell having the appropriate path</u>

<u>assigned thereto from the cell switching unit;</u>

a cell processor to receive and process the ATM cell from the <u>second memory</u> ~~cell switching unit, and to output the ATM cell without going through the cell switching unit~~; and

a third memory to receive and store the ATM cell processed by the cell <u>processor</u> ~~processing unit,~~ and to output the ATM cell without going through the cell switching unit.

12.   (Canceled)

13.   (Currently Amended) The system of claim <u>11</u> ~~12~~, wherein the cell switching unit provides an output to a physical layer and to a loop back, or an output for further processing.

14.   (Currently Amended) The system of claim 13, wherein the cell switching unit adds an end destination field in ~~front of~~ a header of the ATM cell.

15.   (Currently Amended) The system of claim 14, wherein the added end destination field is maintained as the ATM cell passes through the second memory, the cell <u>processor</u> ~~processing unit~~, and the third memory.

16.   (Currently Amended) The system of claim 15, wherein the third memory outputs <u>the ATM cell</u> directly to a physical layer or to a loop back in accordance with <u>information included in</u> the end destination field.

17.   (Original) The system of claim 11, wherein the cell switching unit requires a one virtual path identifier/virtual channel identifier (VPI/VCI) and one type of routing information for any received ATM cell.

18.   (Currently Amended) The system of claim 12, wherein the cell <u>processor</u> ~~processing unit~~ processes the received ATM cell by changing an ATM adaptation layer (AAL) type or by changing payload information.

19-21   (Canceled)

22.   (New) The method of claim 1, wherein processing by the cell processing circuit includes at least one of changing an ATM adaptation layer type or changing payload information.

23.   (New) The method of claim 1, wherein the routing information included in the α Byte identifies one of the following as a destination of the ATM cell: one of a plurality of physical connections or a loop-back path of a network.